

WHAT IS CLAIMED IS:

1. An information handling system, comprising:  
a plurality of processors coupled to a processor bus; and  
5 a memory;  
wherein each of the processors is operable to enter an interrupt mode and be serially released from the interrupt mode so as to reduce contention by the processors for system resources upon release from the interrupt mode.
- 10 2. The information handling system of claim 1, wherein the processor are operable to be serially released from the interrupt mode according to a predetermined delay following the release of each successive processor from the interrupt mode.
- 15 3. The information handling system of claim 1, wherein the interrupt mode is system management interrupt mode.
4. The information handling system of claim 1, wherein the serial release from the interrupt mode reduces contention by the processors for control of the processor bus and memory.
- 20 5. The information handling system of claim 1, wherein the processor assigned to perform the processing tasks associated the interrupt is operable to initiate the release of every other processor from interrupt mode on a timed release basis following the completion by the assigned processor of the processing tasks associated with the interrupt.
- 25 6. The information handling system of claim 5, wherein the processor assigned to perform the processing tasks associated with the interrupt is operable to exit from interrupt mode following the release of every other processor from interrupt mode.

7. A method for exiting from an interrupt mode in a multiple processor computer system, comprising the steps of:

for each processor, identifying whether the processor is the interrupt handling processor assigned to perform the processing tasks necessary for resolving the interrupt or a non-interrupt handling processor not assigned to perform the processing tasks necessary for resolving the interrupt;

for each non-interrupt handling processor, remaining in an interrupt mode until initiated to exit the interrupt mode by the interrupt handling processor;

for the interrupt handling processor, performing the processing tasks necessary for resolving the interrupt; and

for the interrupt handling processor, initiating on a serial basis the exit of each processor from interrupt mode.

8. The method for exiting from an interrupt mode in a multiple processor system of claim 7, further comprising step of:

for the interrupt handling processor, exiting from interrupt mode after each of the non-interrupt handling processors have exited from interrupt mode.

9. The method for exiting from an interrupt mode in a multiple processor system of claim 7, further comprising the step of, for at least each non-interrupt handling processor, setting an indicator associated with each processor to identify that the respective processor is in an interrupt mode.

10. The method for exiting from an interrupt mode in a multiple processor system of claim 9, wherein the step of remaining in an interrupt mode until initiated to exit the interrupt mode comprises the step of remaining in an interrupt mode until the indicator has been reset by the interrupt handling processor.

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11. The method for exiting from an interrupt mode in a multiple processor system of claim 10, further comprising the step of, for each non-interrupt handling processor, identifying whether the processor was in a halt state immediately before entering an interrupt mode.

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12. The method for exiting from an interrupt mode in a multiple processor system of claim 11, further comprising the step of causing to exit from interrupt mode those non-interrupt handling processors identified as being in a halt state immediately before entering an interrupt mode, without respect to whether the indicator has been reset by the interrupt handling processor.

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13. The method for exiting from an interrupt mode in a multiple processor system of claim 10, wherein the indicator for a respective processor is a bit stored in a memory space associated the respective processor.

14. The method for exiting from an interrupt mode in a multiple processor system of claim 13, wherein the step of initiating on a serial basis the exit of each non-interrupt handling processor from interrupt mode comprises the steps of:

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resetting a bit associated with a first non-interrupt handling processor;

pausing for a time period; and

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repeating the steps of resetting and pausing until the interrupt handling processor has initiated the exit of each non-interrupt handling processor from interrupt mode.

15. The method for exiting from an interrupt mode in a multiple processor system of claim 14, wherein the time period is a predetermined time period associated with a time sufficient to permit a processor to exit from an interrupt mode without contention for a processor bus or memory in the computer system.

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16. The method for exiting from an interrupt mode in a multiple processor system of claim 14, wherein the interrupt mode is an interrupt mode associated with a system management interrupt.

17. A method for exiting from an interrupt in a multiple processor computer system, wherein each of the processors are coupled to a processor bus, comprising the steps of:

for each processor, setting an indicator to indicate that the processor is in an interrupt mode;

5 identifying the interrupt handling processor responsible for performing the processing tasks necessary to resolve the interrupt condition;

identifying the non-interrupt handling processors not responsible for performing the processing tasks necessary to resolve the interrupt condition;

10 for each non-interrupt handling processor, determining whether each non-interrupt handling processor was in a halt state immediately before entering the interrupt mode;

for each non-interrupt handling processor, remaining in an interrupt mode until initiated to exit the interrupt mode by the interrupt handling processor;

for the interrupt handling processor, performing the processing tasks necessary to resolve the interrupt condition; and

15 for the interrupt handling processor, initiating the serial exit of the non-interrupt handling processors from interrupt mode, whereby contention by the non-interrupt handling processors for control of the processor bus is reduced.

18. The method for exiting from an interrupt in a multiple processor computer system  
20 of claim 17, wherein the interrupt mode is associated with a system management interrupt.

19. The method for exiting from an interrupt in a multiple processor computer system of claim 17, further comprising the step of, for the interrupt handling processor, exiting from interrupt mode following the exit of each of the non-interrupt handling processors from interrupt mode.

20. The method for exiting from an interrupt in a multiple processor computer system of claim 17, wherein the step of remaining in an interrupt mode until initiated to exit the interrupt mode by the interrupt handling processor comprises the step of remaining in an interrupt mode until the interrupt handling processor resets an indicator as an instruction to the non-interrupt handling processor to exit from the interrupt mode.
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